Rev 2; 10/06

3.3V Single-Piece 1Mb Nonvolatile SRAM with Clock

DS3045W

General Description

The DS3045W consists of a static RAM, a nonvolatile (NV) controller, a year 2000-compliant real-time clock (RTC), and an internal rechargeable manganese lithium (ML) battery. These components are encased in a surface-mount module with a 256-ball BGA footprint. Whenever V_{CC} is applied to the module, it recharges the ML battery, powers the clock and SRAM from the external power source, and allows the contents of the clock registers or SRAM to be modified. When V_{CC} is powered down or out-of-tolerance, the controller write-protects the memory contents and powers the clock and SRAM from the battery. The DS3045W also contains a power-supply monitor output ($\overline{RST}$), as well as a user-programmable interrupt output ($\overline{IRQ}$/FT).

Applications

RAID Systems and Servers
POS Terminals
Industrial Controllers
Data-Acquisition Systems
Gaming
Fire Alarms
PLCs
Routers/Switches

Features

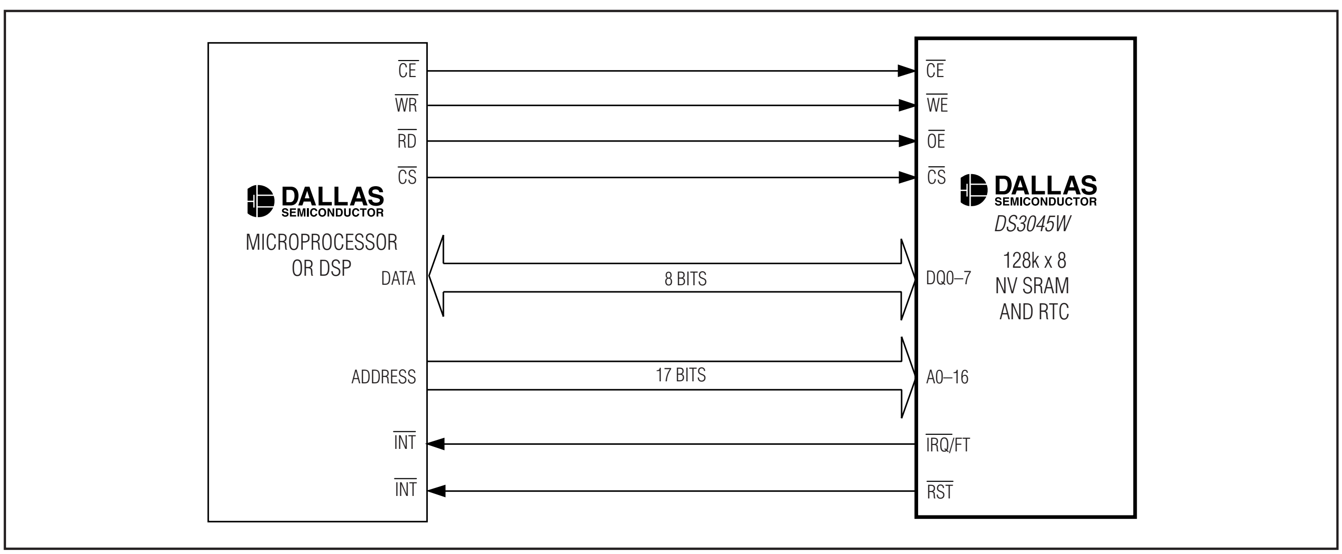
- ♦ **Single-Piece, Reflowable, 27mm x 27mm BGA Package Footprint**
- ♦ **Internal Manganese Lithium Battery and Charger**
- ♦ **Integrated Real-Time Clock**
- ♦ **Unconditionally Write-Protects the Clock and SRAM when V_{CC} is Out-of-Tolerance**
- ♦ **Automatically Switches to Battery Supply when V_{CC} Power Failures Occur**
- ♦ **Reset Output can be Used as a CPU Supervisor**
- ♦ **Interrupt Output can be Used as a CPU Watchdog Timer**
- ♦ **Industrial Temperature Range (-40°C to +85°C)**
- ♦ **UL Recognized**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	SPEED	SUPPLY VOLTAGE
DS3045W-100#	-40°C to +85°C	256-ball 27mm x 27mm BGA Module	100ns	3.3V ±0.3V

#Denotes a RoHS-compliant device that may include lead that is exempt under the RoHS requirements.

Typical Operating Circuit



Pin Configuration appears at end of data sheet.

3.3V Single-Piece 1Mb Nonvolatile SRAM with Clock

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground......-0.3V to +4.6V
Operating Temperature Range ....-40°C to +85°C
Storage Temperature Range ....-40°C to +85°C
Soldering Temperature Range..........See IPC/JEDEC J-STD-020

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		3.0	3.3	3.6	V
Input Logic 1	V_{IH}		2.2		V_{CC}	V
Input Logic 0	V_{IL}		0.0		0.4	V

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.3V ±0.3V, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage Current	I_{IL}		-1.0		+1.0	µA
I/O Leakage Current	I_{IO}	$\overline{CE}$ = $\overline{CS}$ = V_{CC}	-1.0		+1.0	µA
Output-Current High	I_{OH}	At 2.4V	-1.0			mA
Output-Current Low	I_{OL}	At 0.4V	2.0			mA
Output-Current Low $\overline{RST}$	I_{OL} $\overline{RST}$	At 0.4V (Note 1)	8.0			mA
Output-Current Low $\overline{IRQ}$/FT	I_{OL} $\overline{IRQ}$/FT	At 0.4V (Note 1)	7.0			mA
Standby Current	I_{CCS1}	$\overline{CE}$ = $\overline{CS}$ = 2.2V		0.5	7	mA
	I_{CCS2}	$\overline{CE}$ = $\overline{CS}$ = V_{CC} - 0.2V		0.2	5	
Operating Current	I_{CCO1}	t_{RC} = 200ns, outputs open			50	mA
Write Protection Voltage	V_{TP}		2.8	2.9	3.0	V

PIN CAPACITANCE

(T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Capacitance	C_{IN}	Not production tested		15		pF
Input/Output Capacitance	C_{OUT}	Not production tested		15		pF

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.3V ±0.3V, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	DS3045W-100		UNITS
			MIN	MAX	
Read Cycle Time	t_{RC}		100		ns
Access Time	t_{ACC}			100	ns
$\overline{OE}$ to Output Valid	t_{OE}			50	ns
RTC $\overline{OE}$ to Output Valid	t_{OEC}			60	ns
$\overline{CE}$ or $\overline{CS}$ to Output Valid	t_{CO}			100	ns
$\overline{OE}$ or $\overline{CE}$ or $\overline{CS}$ to Output Active	t_{COE}	(Note 2)	5		ns
Output High Impedance from Deselection	t_{OD}	(Note 2)		40	ns
Output Hold from Address	t_{OH}		5		ns
Write Cycle Time	t_{WC}		100		ns
Write Pulse Width	t_{WP}	(Note 3)	75		ns
Address Setup Time	t_{AW}		0		ns
Write Recovery Time	t_{WR1}	(Note 4)	5		ns
	t_{WR2}	(Note 5)	20		
Output High Impedance from $\overline{WE}$	t_{ODW}	(Note 2)		40	ns
Output Active from $\overline{WE}$	t_{OEW}	(Note 2)	5		ns
Data Setup Time	t_{DS}	(Note 6)	40		ns
Data Hold Time	t_{DH1}	(Note 4)	0		ns
	t_{DH2}	(Note 5)	20		
Chip-to-Chip Setup Time	t_{CCS}		40		ns

POWER-DOWN/POWER-UP TIMING

(T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} Fail Detect to $\overline{CE}$, $\overline{CS}$, and $\overline{WE}$ Inactive	t_{PD}	(Note 7)			1.5	µs
V_{CC} Slew from V_{TP} to 0V	t_F		150			µs
V_{CC} Slew from 0V to V_{TP}	t_R		150			µs
V_{CC} Valid to $\overline{CE}$, $\overline{CS}$, and $\overline{WE}$ Inactive	t_{PU}				2	ms
V_{CC} Valid to End of Write Protection	t_{REC}				125	ms
V_{CC} Fail Detect to $\overline{RST}$ Active	t_{RPD}	(Note 1)			3.0	µs
V_{CC} Valid to $\overline{RST}$ Inactive	t_{RPU}	(Note 1)	40	350	525	ms

DATA RETENTION

(T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Expected Data-Retention Time (Per Charge)	t_{DR}	(Notes 7, 8)	2	3		Years

AC TEST CONDITIONS

Input Pulse Levels:	V_{IL} = 0.0V, V_{IH} = 2.7V
Input Pulse Rise and Fall Times:	5ns
Input and Output Timing Reference Level:	1.5V
Output Load:	1 TTL Gate + C_L (100pF) including scope and jig

Note 1: $\overline{IRQ}$/FT and $\overline{RST}$ are open-drain outputs and cannot source current. External pullup resistors should be connected to these pins to realize a logic-high level.

Note 2: These parameters are sampled with a 5pF load and are not 100% tested.

Note 3: t_{WP} is specified as the logical AND of $\overline{CE}$ with $\overline{WE}$ for SRAM writes, or $\overline{CS}$ with $\overline{WE}$ for RTC writes. t_{WP} is measured from the latter of the two related edges going low to the earlier of the two related edges going high.

Note 4: t_{WR1} and t_{DH1} are measured from $\overline{WE}$ going high.

Note 5: t_{WR2} and t_{DH2} are measured from $\overline{CE}$ going high for SRAM writes or $\overline{CS}$ going high for RTC writes.

Note 6: t_{DS} is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high for SRAM writes, or from the earlier of $\overline{CS}$ or $\overline{WE}$ going high for RTC writes.

Note 7: In a power-down condition, the voltage on any pin may not exceed the voltage on V_{CC}.

Note 8: The expected t_{DR} is defined as accumulative time in the absence of V_{CC} starting from the time power is first applied by the user. Minimum expected data-retention time is based upon a maximum of two +230°C convection reflow exposures, followed by a fully charged cell. Full charge occurs with the initial application of V_{CC} for a minimum of 96 hours. This parameter is assured by component selection, process control, and design. It is not measured directly during production testing.

Note 9: $\overline{WE}$ is high for any read cycle.

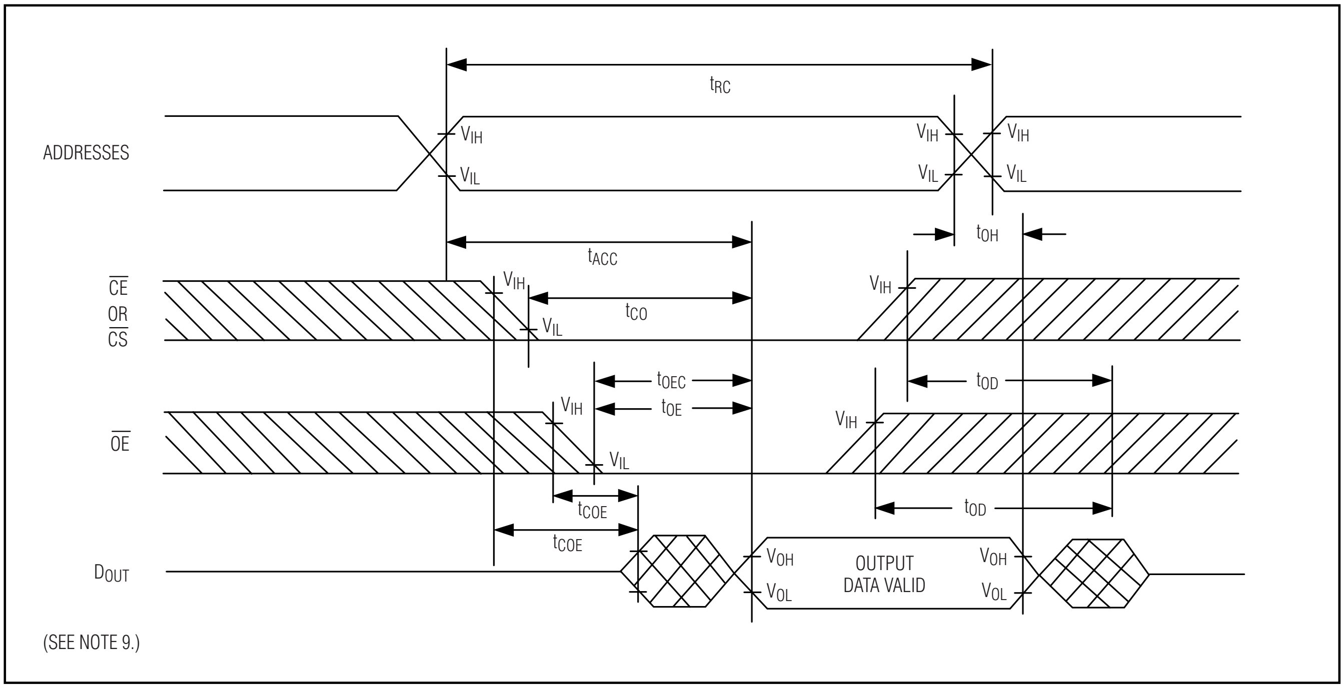
Note 10: $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during write cycle, the output buffers remain in a high-impedance state.

Note 11: If the $\overline{CE}$ or $\overline{CS}$ low transition occurs simultaneously with or latter than the $\overline{WE}$ low transition, the output buffers remain in a high-impedance state during this period.

Note 12: If the $\overline{CE}$ or $\overline{CS}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition, the output buffers remain in a high-impedance state during this period.

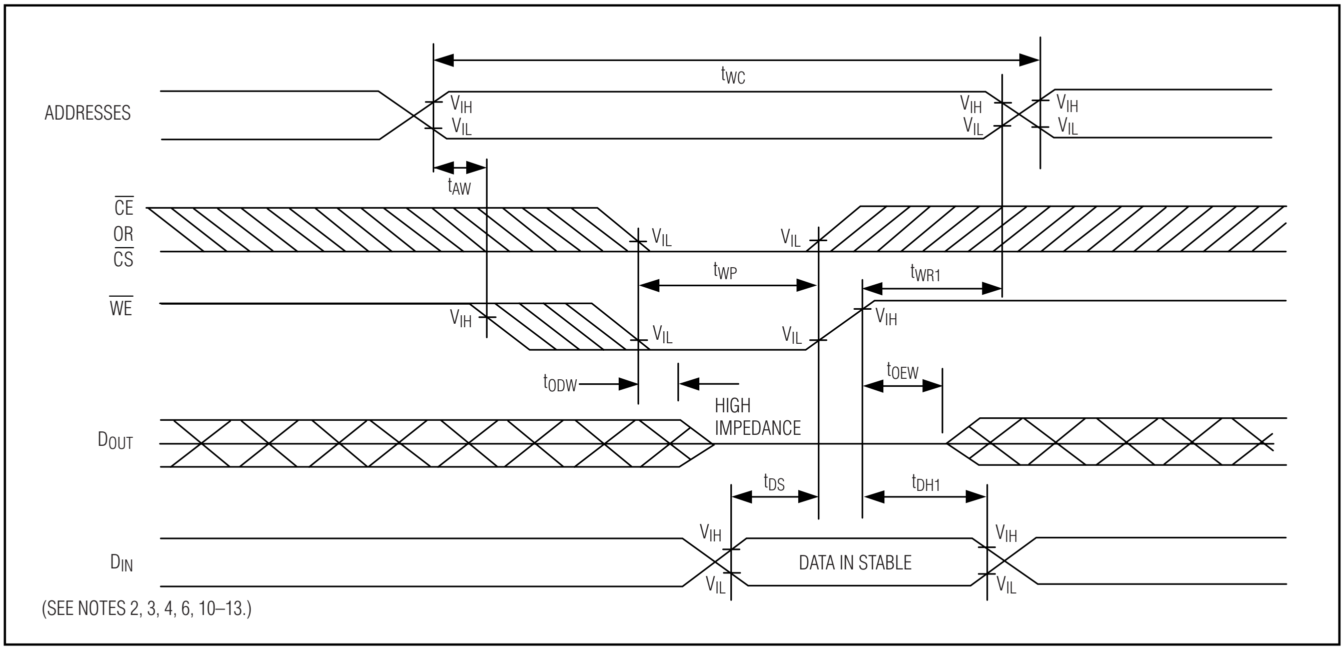
Note 13: If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the related $\overline{CE}$ or $\overline{CS}$ low transition, the output buffers remain in a high-impedance state during this period.

Read Cycle

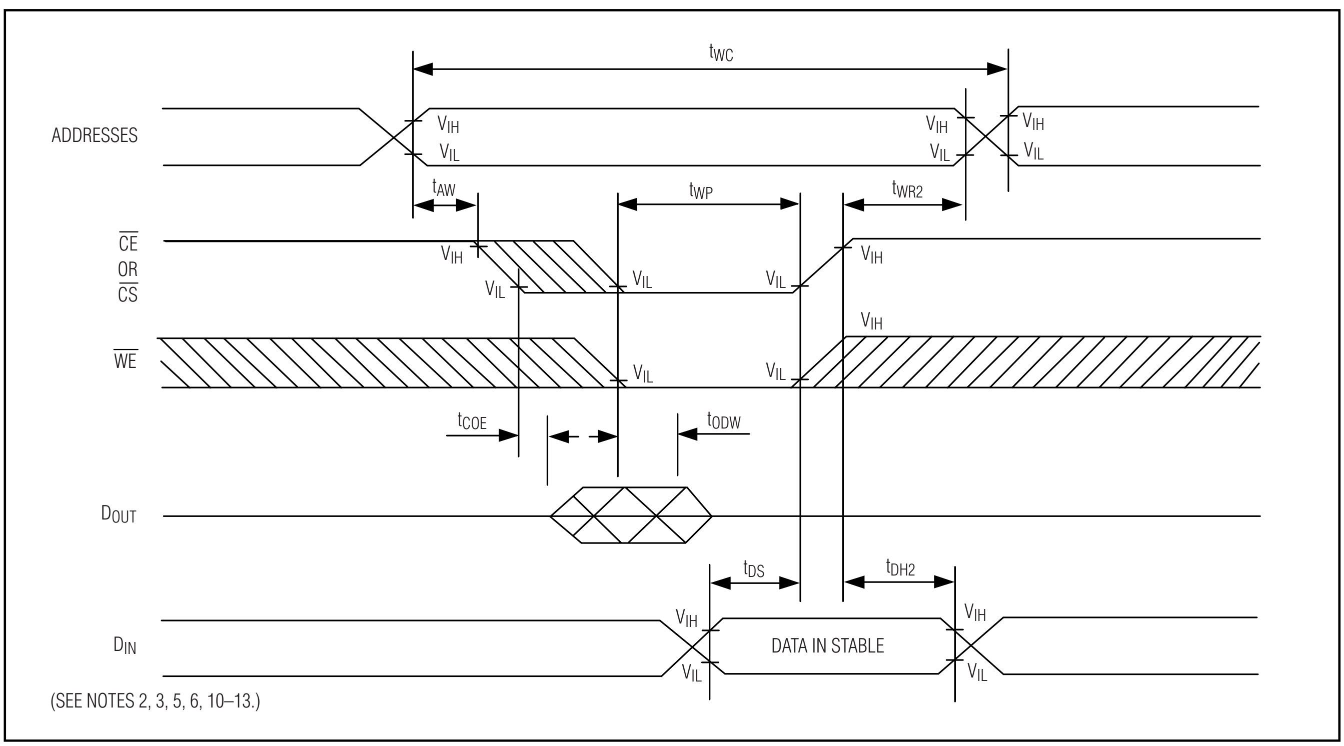


tRC
ADDRESSES
VIH
VIL
VIH
VIL
VIH
VIL
tOH
tACC
CE
OR
CS
VIH
VIL
tCO
VIH
tOEC
tOE
tOD
OE
VIH
VIL
VIH
tCOE
tCOE
tOD
DOUT
VOH
VOL
OUTPUT
DATA VALID
VOH
VOL
(SEE NOTE 9.)

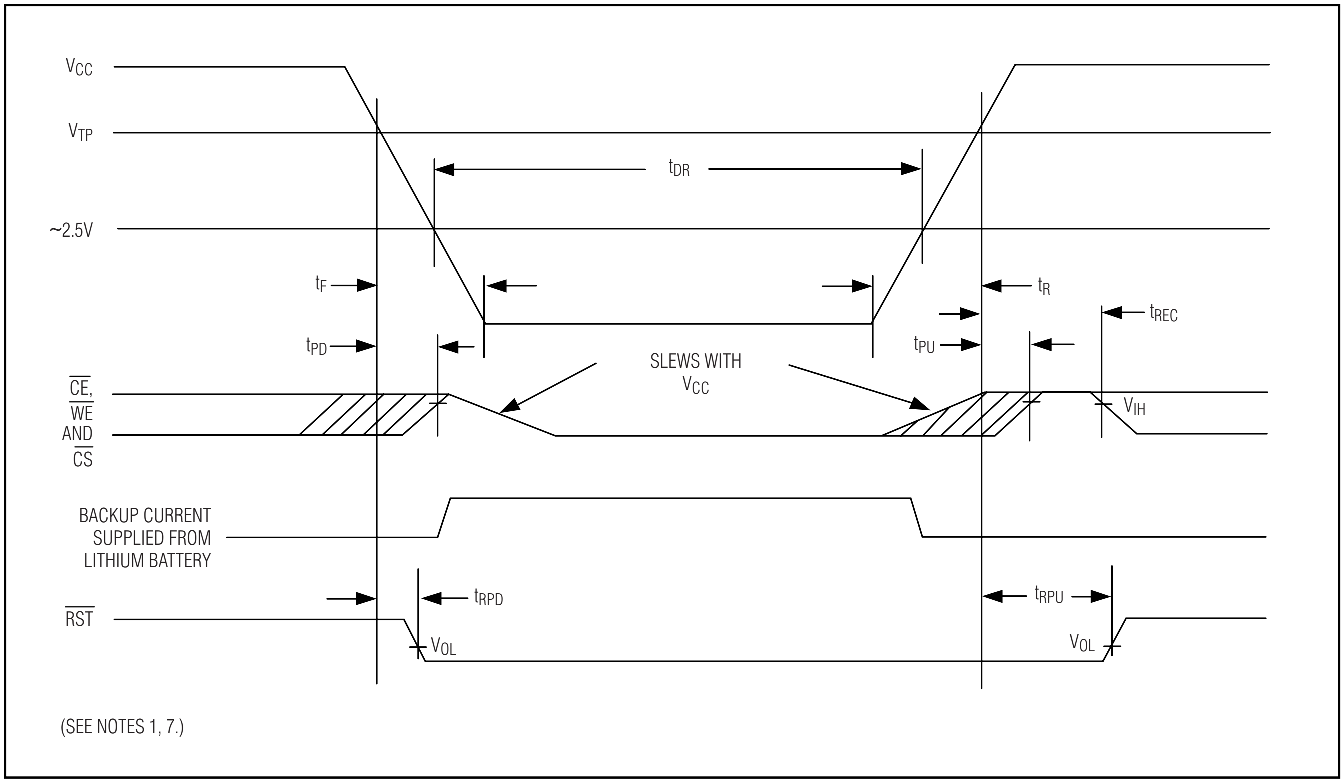
Write Cycle 1



Write Cycle 2

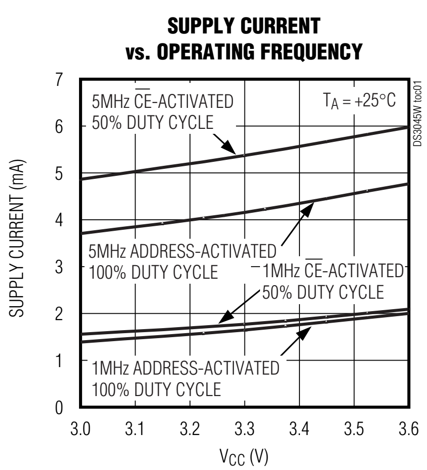


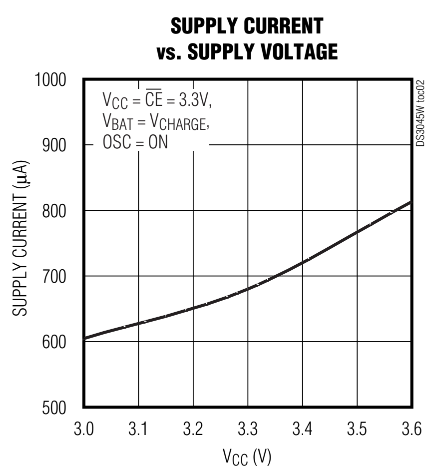
Power-Down/Power-Up Condition

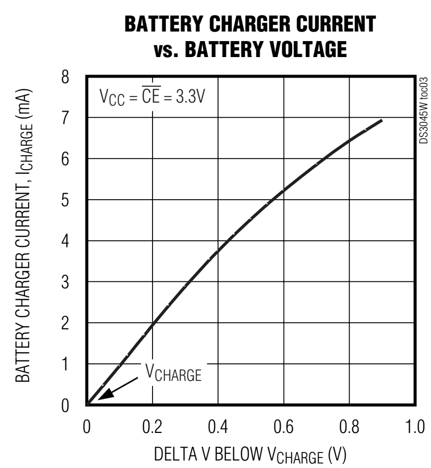


Typical Operating Characteristics

(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)





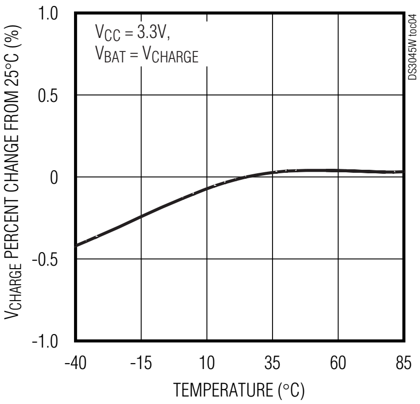


3.3V Single-Piece 1Mb Nonvolatile SRAM with Clock

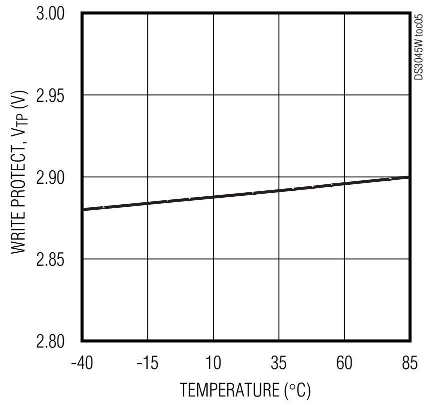
Typical Operating Characteristics (continued)

(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

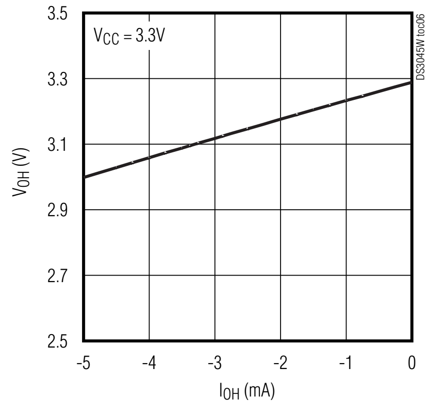
V_{CHARGE} PERCENT CHANGE vs. TEMPERATURE



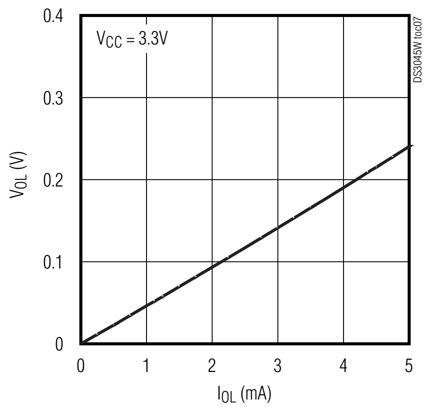
WRITE PROTECTION VOLTAGE vs. TEMPERATURE



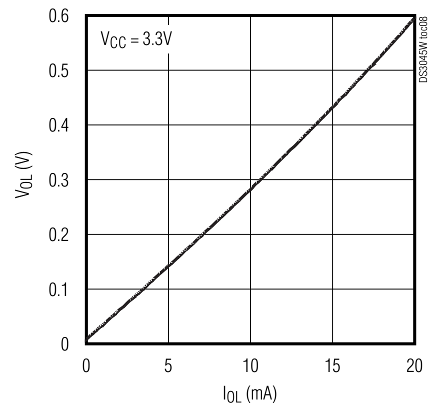
DQ OUTPUT-VOLTAGE HIGH vs. DQ OUTPUT-CURRENT HIGH



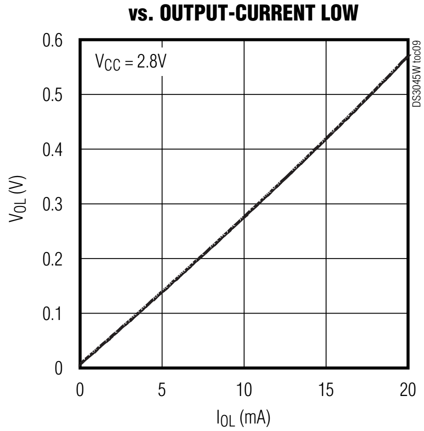
DQ OUTPUT-VOLTAGE LOW vs. DQ OUTPUT-CURRENT LOW



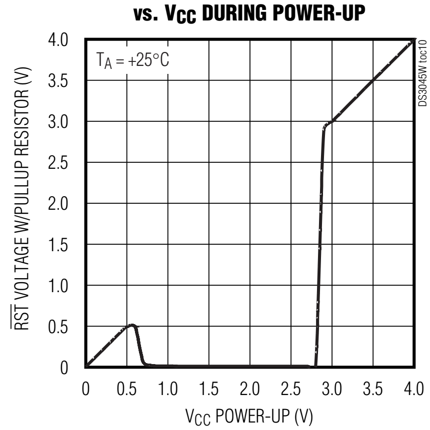
$\overline{IRQ}$/FT OUTPUT-VOLTAGE LOW vs. OUTPUT-CURRENT LOW



$\overline{RST}$ OUTPUT-VOLTAGE LOW vs. OUTPUT-CURRENT LOW



$\overline{RST}$ VOLTAGE vs. V_{CC} DURING POWER-UP

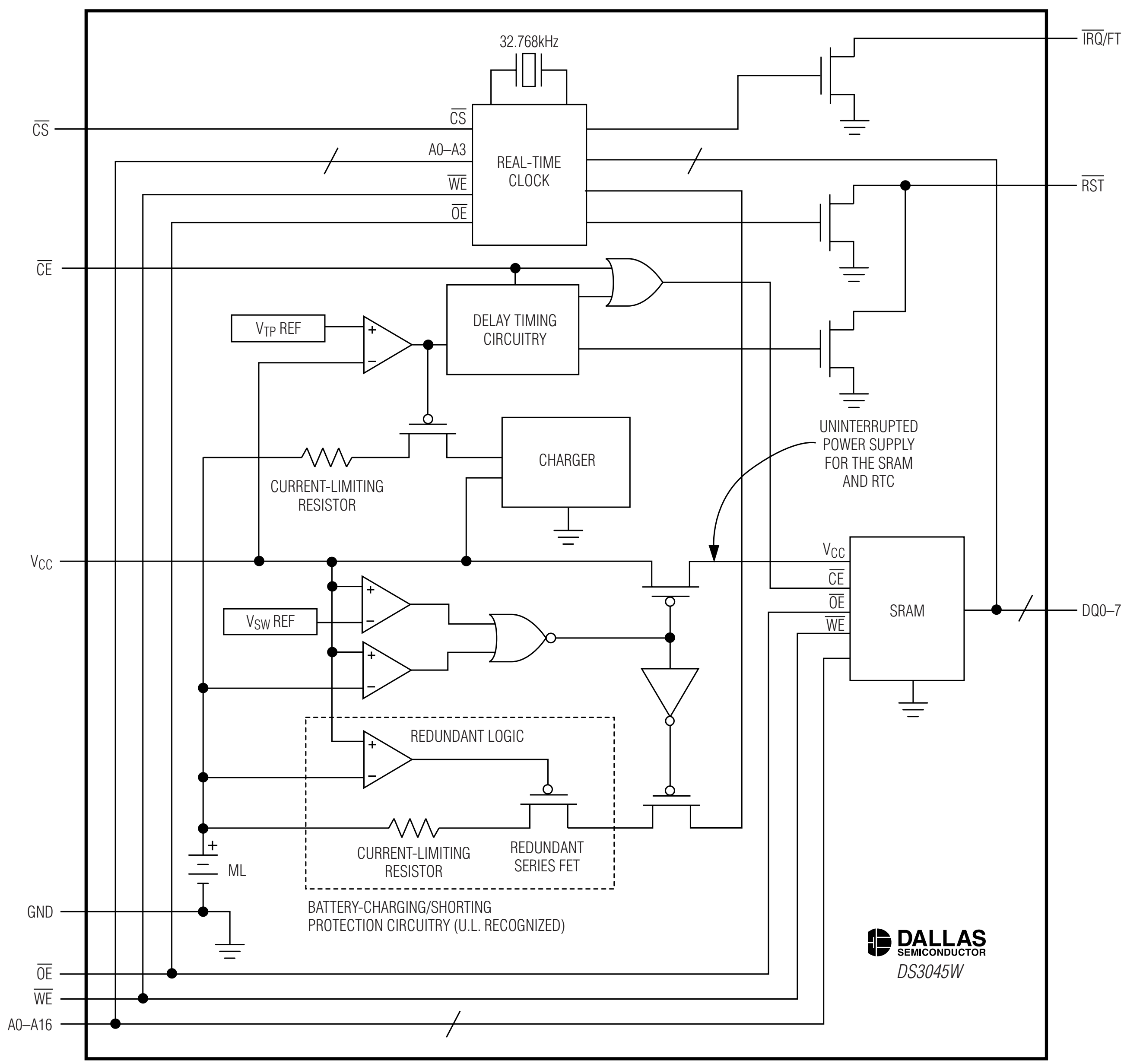


Pin Description

BALLS	NAME	DESCRIPTION
A1, A2, A3, A4	GND	Ground
B1, B2, B3, B4	$\overline{\text{IRQ}}$/FT	Interrupt/Frequency Test Output
C1, C2, C3, C4	A15	Address Input 15
D1, D2, D3, D4	A16	Address Input 16
E1, E2, E3, E4	$\overline{\text{RST}}$	Reset Output
F1, F2, F3, F4	V_{CC}	Supply Voltage
G1, G2, G3, G4	$\overline{\text{WE}}$	Write Enable Input
H1, H2, H3, H4	$\overline{\text{OE}}$	Output Enable Input
J1, J2, J3, J4	$\overline{\text{CE}}$	SRAM Chip Enable Input
K1, K2, K3, K4	DQ7	Data Input/Output 7
L1, L2, L3, L4	DQ6	Data Input/Output 6
M1, M2, M3, M4	DQ5	Data Input/Output 5
N1, N2, N3, N4	DQ4	Data Input/Output 4
P1, P2, P3, P4	DQ3	Data Input/Output 3
R1, R2, R3, R4	DQ2	Data Input/Output 2
T1, T2, T3, T4	DQ1	Data Input/Output 1
U1, U2, U3, U4	DQ0	Data Input/Output 0
V1, V2, V3, V4	GND	Ground
W1, W2, W3, W4	GND	Ground
Y1, Y2, Y3, Y4	GND	Ground
A17, A18, A19, A20	GND	Ground
B17, B18, B19, B20	N.C.	No Connection
C17,C18,C19, C20	N.C.	No Connection
D17, D18, D19, D20	A14	Address Input 14
E17, E18, E19, E20	A13	Address Input 13
F17, F18, F19, F20	A12	Address Input 12
G17, G18, G19, G20	A11	Address Input 11
H17, H18, H19, H20	A10	Address Input 10
J17, J18, J19, J20	A9	Address Input 9
K17, K18, K19, K20	A8	Address Input 8
L17, L18, L19, L20	A7	Address Input 7
M17, M18, M19, M20	A6	Address Input 6
N17, N18, N19, N20	A5	Address Input 5
P17, P18, P19, P20	A4	Address Input 4
R17, R18, R19, R20	A3	Address Input 3
T17, T18, T19, T20	A2	Address Input 2
U17, U18, U19, U20	A1	Address Input 1
V17, V18, V19, V20	A0	Address Input 0
W17, W18, W19, W20	GND	Ground
Y17, Y18, Y19, Y20	GND	Ground
A5, B5, C5, D5	N.C.	No Connection
A6, B6, C6, D6	N.C.	No Connection
A7, B7, C7, D7	N.C.	No Connection
A8, B8, C8, D8	N.C.	No Connection
A9, B9, C9, D9	N.C.	No Connection
A10, B10, C10, D10	V_{CC}	Supply Voltage
A11, B11, C11, D11	N.C.	No Connection
A12, B12, C12, D12	N.C.	No Connection
A13, B13, C13, D13	N.C.	No Connection
A14, B14, C14, D14	N.C.	No Connection
A15, B15, C15, D15	N.C.	No Connection
A16, B16, C16, D16	N.C.	No Connection
U5, V5, W5, Y5	$\overline{\text{CS}}$	RTC Chip Select Input
U6, V6, W6, Y6	N.C.	No Connection
U7, V7, W7, Y7	N.C.	No Connection
U8, V8, W8, Y8	N.C.	No Connection
U9, V9, W9, Y9	N.C.	No Connection
U10, V10, W10, Y10	N.C.	No Connection
U11, V11, W11, Y11	N.C.	No Connection
U12, V12, W12, Y12	N.C.	No Connection
U13, V13, W13, Y13	N.C.	No Connection
U14, V14, W14, Y14	N.C.	No Connection
U15, V15, W15, Y15	N.C.	No Connection
U16, V16, W16, Y16	N.C.	No Connection

3.3V Single-Piece 1Mb Nonvolatile SRAM with Clock

Functional Diagram



Detailed Description

The DS3045W is a 1Mb (128k x 8 bits) fully static, NV memory similar in function and organization to the DS1245W NV SRAM, but also containing an RTC and rechargeable ML battery. The DS3045W NV SRAM constantly monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent data corruption. There is no limit to the number of write cycles that can be executed, and no additional support circuitry is required for microprocessor interfacing. This device can be used in place of SRAM, EEPROM, or flash components.

User access to either the SRAM or the real-time clock registers is accomplished with a byte-wide interface and discrete control inputs, allowing for a direct interface to many 3.3V microprocessor devices.

The DS3045W RTC contains a full-function, year 2000-compliant (Y2KC) clock/calendar with an RTC alarm, watchdog timer, battery monitor, and power monitor. RTC registers contain century, year, month, date, day, hours, minutes, and seconds data in a 24-hour BCD format. Corrections for day of the month and leap year are made automatically.

The DS3045W RTC registers are double-buffered into an internal and external set. The user has direct access to the external set. Clock/calendar updates to the external set of registers can be disabled and enabled to allow the user to access static data. Assuming the internal oscillator is on, the internal registers are continually updated, regardless of the state of the external registers, assuring that accurate RTC information is always maintained.

The DS3045W contains interrupt ($\overline{IRQ}$/FT) and reset ($\overline{RST}$) outputs, which can be used to control CPU activity. The $\overline{IRQ}$/FT interrupt output can be used to generate an external interrupt when the RTC register values match user-programmed alarm values. The interrupt is always available while the device is powered from the system supply, and it can be programmed to occur when in the battery-backed state to serve as a system wake-up. The $\overline{IRQ}$/FT output can also be used as a CPU watchdog timer. CPU activity is monitored and an interrupt can be activated if the correct activity is not detected. The $\overline{RST}$ output can be used to detect a system power-down or failure and hold the CPU in a safe state until normal power returns.

The DS3045W constantly monitors the voltage of the internal battery. The battery-low flag (BLF) in the RTC FLAGS register is not writeable and should always be a 0 when read. Should a 1 ever be present, the battery voltage is below ~2V and the contents of the clock and SRAM are questionable.

The DS3045W module is constructed on a standard 256-ball, 27mm x 27mm BGA substrate. Unlike other surface-mount NV memory modules that require the battery to be removable for soldering, the internal ML battery can tolerate exposure to convection reflow soldering temperatures, allowing this single-piece component to be handled with standard BGA assembly techniques.

Table 1. RTC/Memory Operational Truth Table

$\overline{CS}$	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	MODE	ICC	OUTPUTS
0	1	1	0	RTC Read	Active	Active
0	1	1	1	RTC Read	Active	High Impedance
0	0	1	X	RTC Write	Active	High Impedance
1	1	0	0	SRAM Read	Active	Active
1	1	0	1	SRAM Read	Active	High Impedance
1	0	0	X	SRAM Write	Active	High Impedance
1	X	1	X	Standby	Standby	High Impedance
0	X	0	X	Invalid (1)	Active	Invalid

X = Don't care. (1) = See Figure 4.

SRAM Read Mode

The DS3045W executes an SRAM read cycle whenever $\overline{CS}$ (RTC chip select) and $\overline{WE}$ (write enable) are inactive (high) and $\overline{CE}$ (SRAM chip enable) is active (low). The unique address specified by the 17 address inputs (A0 to A16) defines which of the 131,072 bytes of SRAM data is to be accessed. Valid data will be available to the eight data output drivers within t_{ACC} (access time) after the last address input signal is stable, providing that $\overline{CE}$ and $\overline{OE}$ (output enable) access times are also satisfied. If $\overline{CE}$ and $\overline{OE}$ access times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access.

SRAM Write Mode

The DS3045W executes an SRAM write cycle whenever $\overline{CS}$ is inactive (high) and the $\overline{CE}$ and $\overline{WE}$ signals are active (low) after address inputs are stable. The later-occurring falling edge of $\overline{CE}$ or $\overline{WE}$ determines the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{CS}$ and $\overline{OE}$ control signal should be kept inactive (high) during SRAM write cycles to avoid bus contention. However, if the output drivers have been enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ disables the outputs in t_{ODW} from its falling edge.

Clock Operations

Table 2. RTC Register Map

ADDRESS	DATA								FUNCTION/RANGE	
	B7	B6	B5	B4	B3	B2	B1	B0		
xxxxFh	10 YEAR				YEAR				YEAR	00–99
xxxxEh	X	X	X	10 M	MONTH				MONTH	01–12
xxxxDh	X	X	10 DATE		DATE				DATE	01–31
xxxxCh	X	FT	X	X	X	DAY			DAY	01–07
xxxxBh	X	X	10 HOUR		HOUR				HOUR	00–23
xxxxAh	X	10 MINUTES			MINUTES				MINUTES	00–59
xxxx9h	$\overline{OSC}$	10 SECONDS			SECONDS				SECONDS	00–59
xxxx8h	W	R	10 CENTURY		CENTURY				CONTROL	00–39
xxxx7h	WDS	BMB4	BMB3	BMB2	BMB1	BMB0	RB1	RB0	WATCHDOG	—
xxxx6h	AE	Y	ABE	Y	Y	Y	Y	Y	INTERRUPTS	—
xxxx5h	AM4	Y	10 DATE		DATE				ALARM DATE	01–31
xxxx4h	AM3	Y	10 HOURS		HOURS				ALARM HOURS	00–23
xxxx3h	AM2	10 MINUTES			MINUTES				ALARM MINUTES	00–59
xxxx2h	AM1	10 SECONDS			SECONDS				ALARM SECONDS	00–59
xxxx1h	Y	Y	Y	Y	Y	Y	Y	Y	UNUSED	—
xxxx0h	WF	AF	0	BLF	0	0	0	0	FLAGS	—

x = Don't care address bits.
X = Unused. Read/writeable under write and read bit control.
FT = Frequency test bit.
$\overline{OSC}$ = Oscillator start/stop bit.
W = Write bit.
R = Read bit.
WDS = Watchdog steering bit.
BMB0–BMB4 = Watchdog multiplier bits.
RB0, RB1 = Watchdog resolution bits.
AE = Alarm flag enable.
Y = Unused. Read/writeable without write and read bit control.
ABE = Alarm in backup mode enable.
AM1–AM4 = Alarm mask bits.
WF = Watchdog flag.
AF = Alarm flag.
0 = Reads as a 0 and cannot be changed.
BLF = Battery low flag.

RTC Read Mode

The DS3045W executes an RTC read cycle whenever $\overline{CE}$ (SRAM chip enable) and WE (write enable) are inactive (high) and $\overline{CS}$ (RTC chip select) is active (low). The least significant 4 address inputs (A0 to A3) define which of the 16 RTC registers is to be accessed (see Table 2). Valid data is available to the eight data output drivers within t_{ACC} (access time) after the last address input signal is stable, providing that $\overline{CS}$ and $\overline{OE}$ (output enable) access times are also satisfied. If $\overline{CS}$ and $\overline{OE}$ access times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CS}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CS}$ or t_{OEC} for $\overline{OE}$ rather than address access.

RTC Write Mode

The DS3045W executes an RTC write cycle whenever $\overline{CE}$ is inactive (high) and the $\overline{CS}$ and $\overline{WE}$ signals are active (low) after address inputs are stable. The later-occurring falling edge of $\overline{CS}$ or $\overline{WE}$ determines the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CS}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{CE}$ and $\overline{OE}$ control signals should be kept inactive (high) during RTC write cycles to avoid bus contention. However, if the output drivers have been enabled ($\overline{CS}$ and $\overline{OE}$ active) then $\overline{WE}$ disables the outputs in t_{ODW} from its falling edge.

Clock Oscillator Mode

The oscillator can be turned off to minimize battery current drain. The $\overline{OSC}$ bit is the MSB of the SECONDS register, and must be initialized to a 0 to start the oscillator upon first power application. The $\overline{OSC}$ bit is factory set to a 1 prior to shipment. Oscillator operation and frequency can be verified by setting the FT bit to a 1 and monitoring the $\overline{IRQ}$/FT output for 512Hz.

Reading the Clock

When reading the RTC data, it is recommended to halt updates to the external set of double-buffered RTC registers. This puts the external registers into a static state, allowing the data to be read without register values changing during the read process. Normal updates to the internal registers continue while in this state. External updates are halted by writing a 1 to the read bit (R). As long as a 1 remains in the R bit, updating is inhibited. After a halt is issued, the registers reflect the RTC count (day, date, and time) that was current at the moment the halt command was issued. Normal updates to the external set of registers resume within 1 second after the R bit is set to a 0 for a minimum of 500µs. The R bit must be a 0 for a minimum of 500µs to ensure the external registers have fully updated.

Setting the Clock

As with a clock read, it is also recommended to halt updates prior to setting new time values. Setting the write bit (W) to a 1 halts updates of the external RTC registers 8h to Fh. After setting the W bit to a 1, the RTC registers can be loaded with the desired count (day, date, and time) in BCD format. Setting the W bit to a 0 then transfers the values written to the internal registers and allows normal clock operation to resume.

Frequency Test Mode

The DS3045W frequency test mode uses the $\overline{IRQ}$/FT open-drain output. With the oscillator running, the $\overline{IRQ}$/FT output toggles at 512Hz when the FT bit is a 1, the alarm-flag enable bit (AE) is a 0, and the watchdog-enable bit (WDS) is a 1 or the WATCHDOG register is written to 00h (FT • $\overline{AE}$ • (WDS + $\overline{WATCHDOG}$)). The $\overline{IRQ}$/FT output and the frequency test mode can be used to measure the actual frequency of the 32.768kHz RTC oscillator. The FT bit is reset to a 0 on power-up.

Using the Clock Alarm

The alarm settings and control for the DS3045W reside within RTC registers 2h–5h. The INTERRUPTS register (6h) contains two alarm-enable bits: alarm enable (AE) and alarm in backup enable (ABE). The AE and ABE bits must be set as described below for the $\overline{IRQ}$/FT output to be activated when an alarm match occurs.

The alarm can be programmed to activate on a specific day of the month or repeat every day, hour, minute, or second. It can also be programmed to go off while the DS3045W is in the Data Retention Mode to serve as a system wake-up. Alarm mask bits AM1 to AM4 control the alarm mode (see Table 3). Configurations not listed in the table will default to the once-per-second mode to notify the user of an incorrect alarm setting.

Table 3. Alarm Mask Bits

AM4	AM3	AM2	AM1	ALARM RATE
1	1	1	1	Once per second
1	1	1	0	When seconds match
1	1	0	0	When minutes and seconds match
1	0	0	0	When hours, minutes, and seconds match
0	0	0	0	When date, hours, minutes, and seconds match

When the RTC register values match alarm register settings, the alarm flag (AF) is set to a 1. If AE is also a 1, the alarm condition activates the $\overline{IRQ}$/FT output. When $\overline{CS}$ is active, the $\overline{IRQ}$/FT signal can be cleared by holding the FLAGS register address stable for t_{RC} and forcing either $\overline{OE}$ or $\overline{WE}$ active (see Figure 1). The flag does not change state until the end of the read/write cycle and after the $\overline{IRQ}$/FT signal has deasserted. To avoid inadvertently clearing the $\overline{IRQ}$/FT signal while preparing for subsequent write/read cycles at other register addresses, assure that t_{AW} is met for that subsequent address (see Figure 2).

The $\overline{IRQ}$/FT output can also be activated during battery backup mode. The $\overline{IRQ}$/FT goes low if an alarm occurs and both AE and ABE are set to 1. The AE and ABE bits are reset to 0 during the power-up transition, but an alarm generated during power-up will set AF to a 1. Therefore, the AF bit can be read after system power-up to determine if an alarm was generated during the power-up sequence. Figure 3 illustrates alarm timing during battery backup mode and power-up states.

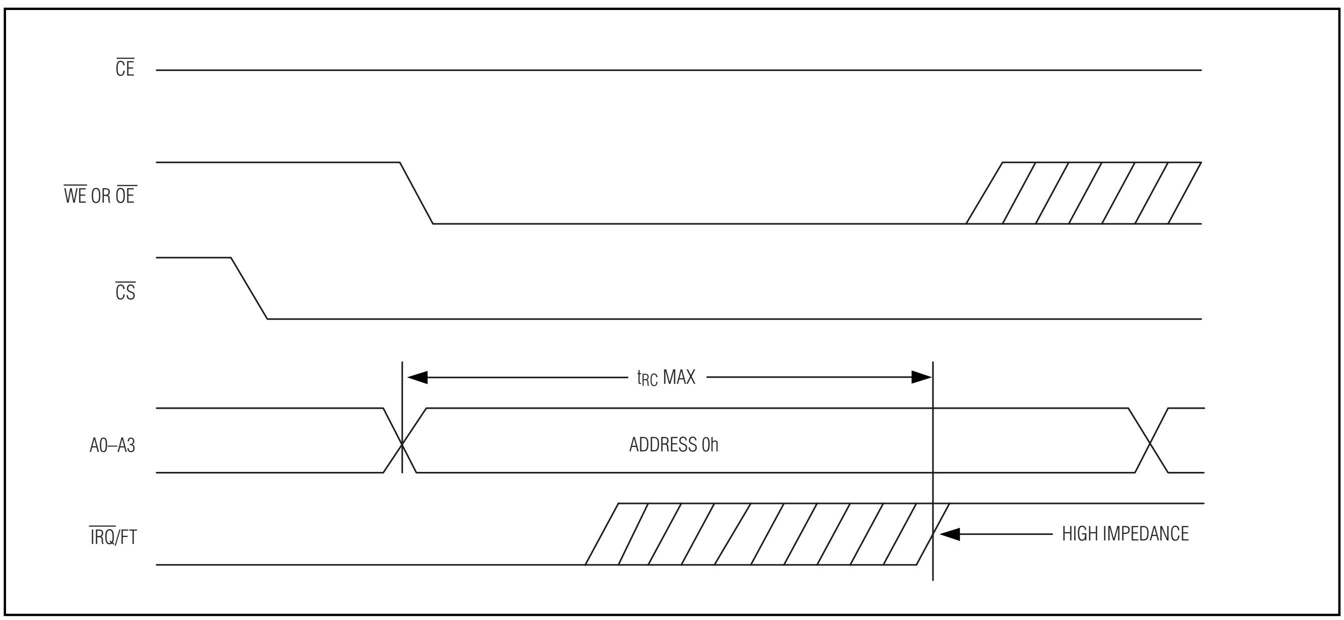


Figure 1. Clearing Active IRQ Waveforms

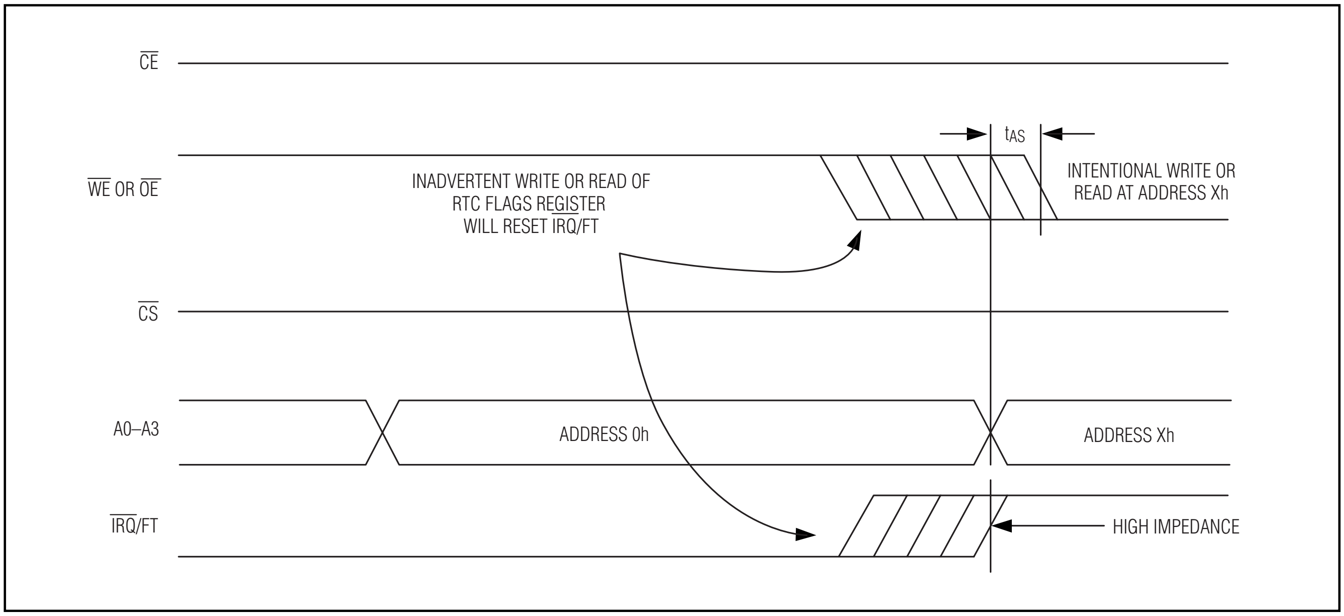


Figure 2. Prevent Accidental Clearing of IRQ Waveforms

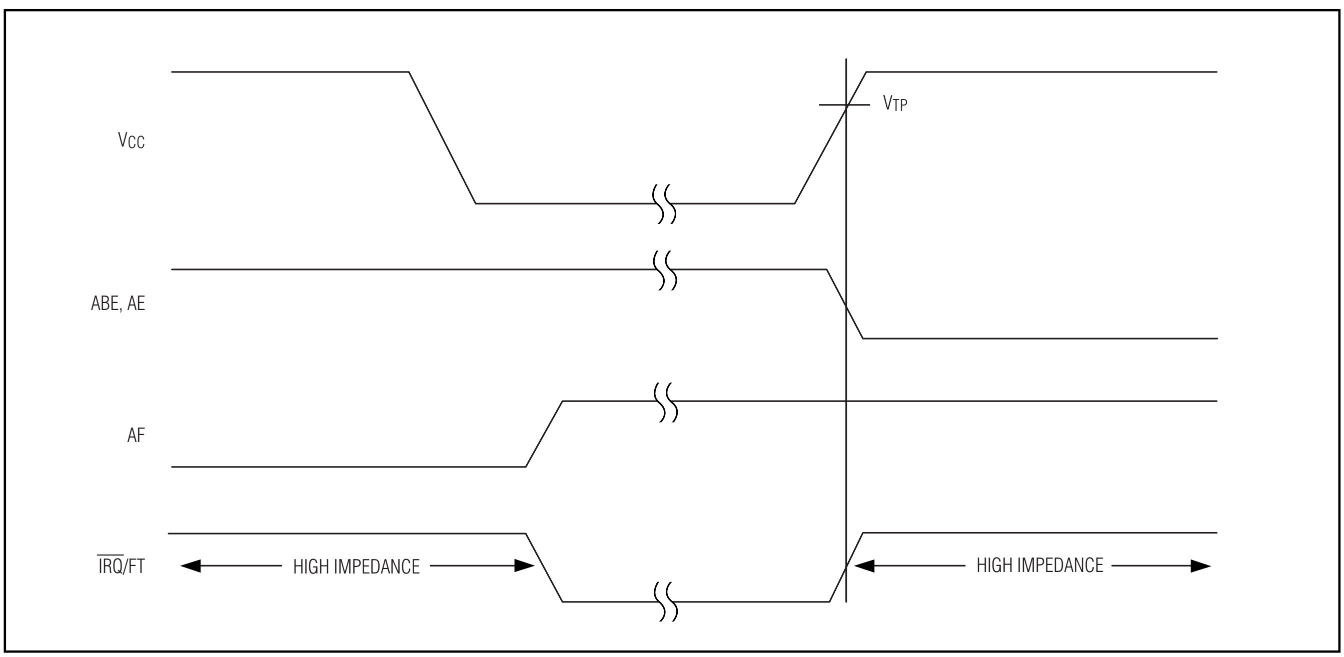


Figure 3. Battery Backup Mode Alarm Waveforms

3.3V Single-Piece 1Mb Nonvolatile SRAM with Clock

Using the Watchdog Timer

The watchdog timer can be used to detect an out-of-control processor. The user programs the watchdog timer by setting the desired timeout delay into the WATCHDOG register. The five high-order WATCHDOG register bits store a binary multiplier and the two lower-order WATCHDOG bits select the resolution, where 00 = $^1/_{16}$ second, 01 = $^1/_4$ second, 10 = 1 second, and 11 = 4 seconds. The watchdog timeout value is then determined by multiplication of the 5-bit multiplier value with the 2-bit resolution value. (For example: writing 00001110 (0Eh) into the WATCHDOG register = 3 x 1 second, or 3 seconds.) If the processor does not reset the timer within the specified period, the watchdog flag (WF) is set to a 1 and a processor interrupt is generated and stays active until either WF is read or the WATCHDOG register is read or written.

The MSB of the WATCHDOG register is the watchdog steering bit (WDS). When WDS is set to a 0, the watchdog activates the $\overline{\text{IRQ}}$/FT output when the watchdog times out. WDS should not be written to a 1, and should be initialized to a 0 if the watchdog function is enabled.

The watchdog timer resets when the processor performs a read or write of the WATCHDOG register. The timeout period then starts over. The watchdog timer is disabled by writing a value of 00h to the WATCHDOG register. The watchdog function is automatically disabled upon power-up and the WATCHDOG register is cleared to 00h.

Clock Accuracy

The DS3045W module is trimmed at the factory to an accuracy of 1 minute per month at +25°C.

Power-On Default States

Upon each application of power to the device, the following register bits are automatically set to 0:

WDS = 0, BMB0–BMB4 = 0, RB0 = 0, RB1 = 0, AE = 0, ABE = 0.

All other RTC bits are undefined.

Data-Retention Mode

The DS3045W provides full functional capability for V_{CC} greater than 3.0V and write-protects by 2.8V. Data is maintained in the absence of V_{CC} without additional support circuitry. The NV SRAM constantly monitors V_{CC}. Should the supply voltage decay, the NV SRAM automatically write-protects itself. All inputs become don't care, and all data outputs become high impedance. As V_{CC} falls below approximately 2.5V (V_{SW}), the power-switching circuit connects the lithium energy source to the clock and SRAM to maintain time and retain data. During power-up, when V_{CC} rises above V_{SW}, the power-switching circuit connects external V_{CC} to the clock and SRAM, and disconnects the lithium energy source. Normal clock or SRAM operation can resume after V_{CC} exceeds V_{TP} for a minimum duration of t_{REC}.

Battery Charging

When V_{CC} is greater than V_{TP} an internal regulator will charge the battery. The UL-approved charger circuit includes short-circuit protection and a temperature-stabilized voltage reference for on-demand charging of the internal battery. Typical data retention expectations greater than 2 years per charge cycle are achievable.

A maximum of 96 hours of charging time is required to fully charge a depleted battery.

System Power Monitoring

When the external V_{CC} supply falls below the selected out-of-tolerance trip point, the output $\overline{\text{RST}}$ is forced active (low). Once active, the $\overline{\text{RST}}$ is held active until the V_{CC} supply has fallen below that of the internal battery. On power-up, the $\overline{\text{RST}}$ output is held active until the external supply is greater than the selected trip point and one reset timeout period (t_{RPU}) has elapsed. This is sufficiently longer than t_{REC} to ensure that the RTC and SRAM are ready for access by the microprocessor.

Freshness Seal and Shipping

The DS3045W is shipped from Dallas Semiconductor with the RTC oscillator disabled and the lithium battery electrically disconnected, guaranteeing that no battery capacity has been consumed during transit or storage. As shipped, the lithium battery is ~60% charged, and no pre-assembly charging operations should be attempted.

When V_{CC} is first applied at a level greater than V_{TP}, the lithium battery is enabled for backup operation. The user is required to enable the oscillator (MSB of SECONDS register) and initialize the required RTC registers for proper timekeeping operation. A 96 hour initial battery charge time is recommended for new system installations.

Applications Information

Power-Supply Decoupling

To achieve the best results when using the DS3045W, assure that all V_{CC} and GND balls are connected and decouple the power supply with a 0.1µF capacitor. Use a high-quality, ceramic surface-mount capacitor if possible. Surface-mount components minimize lead inductance, which improves performance, and ceramic capacitors tend to have adequate high-frequency response for decoupling applications.

Avoiding Data Bus Contention

Care should be taken to avoid simultaneous access of the SRAM and RTC devices (see Figure 4). Any chip-enable overlap violates t_{CCS} and can result in invalid and unpredictable behavior.

Using the Open-Drain $\overline{IRQ}$/FT and $\overline{RST}$ Outputs

The $\overline{IRQ}$/FT and $\overline{RST}$ outputs are open drain, and therefore require pullup resistors to realize a high logic output level. Pullup resistor values between 1kΩ and 10kΩ are typical.

Battery Charging/Lifetime

The DS3045W charges an ML battery to maximum capacity in approximately 96 hours of operation when V_{CC} is greater than V_{TP}. Once the battery is charged, its lifetime depends primarily on the V_{CC} duty cycle. The DS3045W can maintain data from a single, initial charge for up to 2 years. Once recharged, this deep-discharge cycle can be repeated for up to 20 times, producing a worst-case service life of 40 years. More typical duty cycles are of shorter duration, enabling the DS3045W to be charged hundreds of times, and extending the service life well beyond 40 years.

Recommended Cleaning Procedures

The DS3045W can be cleaned using aqueous-based cleaning solutions. No special precautions are needed when cleaning boards containing a DS3045W module.

Removal of the topside label violates the environmental integrity of the package and voids the warranty of the product.

Recommended Reflow Temperature Profile

PROFILE FEATURE	Sn-Pb EUTECTIC ASSEMBLY
Average Ramp-Up Rate (T_L to T_P)	3°C/Second Max
Preheat - Temperature Min (T_{Smin}) - Temperature Max (T_{Smax}) - Time (Min to Max) (ts)	 100°C 150°C 60 to 120 Seconds
T_{Smax} to T_L - Ramp-Up Rate	
Time maintained above: - Temperature (T_L) - Time (t_L)	 +183°C 60 to 150 Seconds
Peak Temperature (T_P)	225 +0/-5°C
Time Within 5°C of Actual Peak Temperature (T_P)	10 to 30 Seconds
Ramp-Down Rate	6°C/Second Max
Time 25°C to Peak Temperature	6 Minutes Max

Note: *All temperatures refer to topside of the package, measured on the package body surface.*

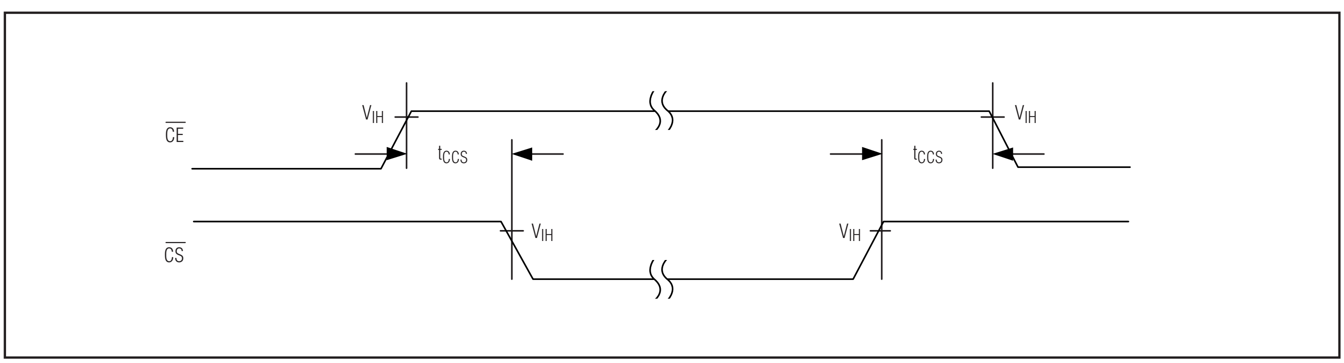
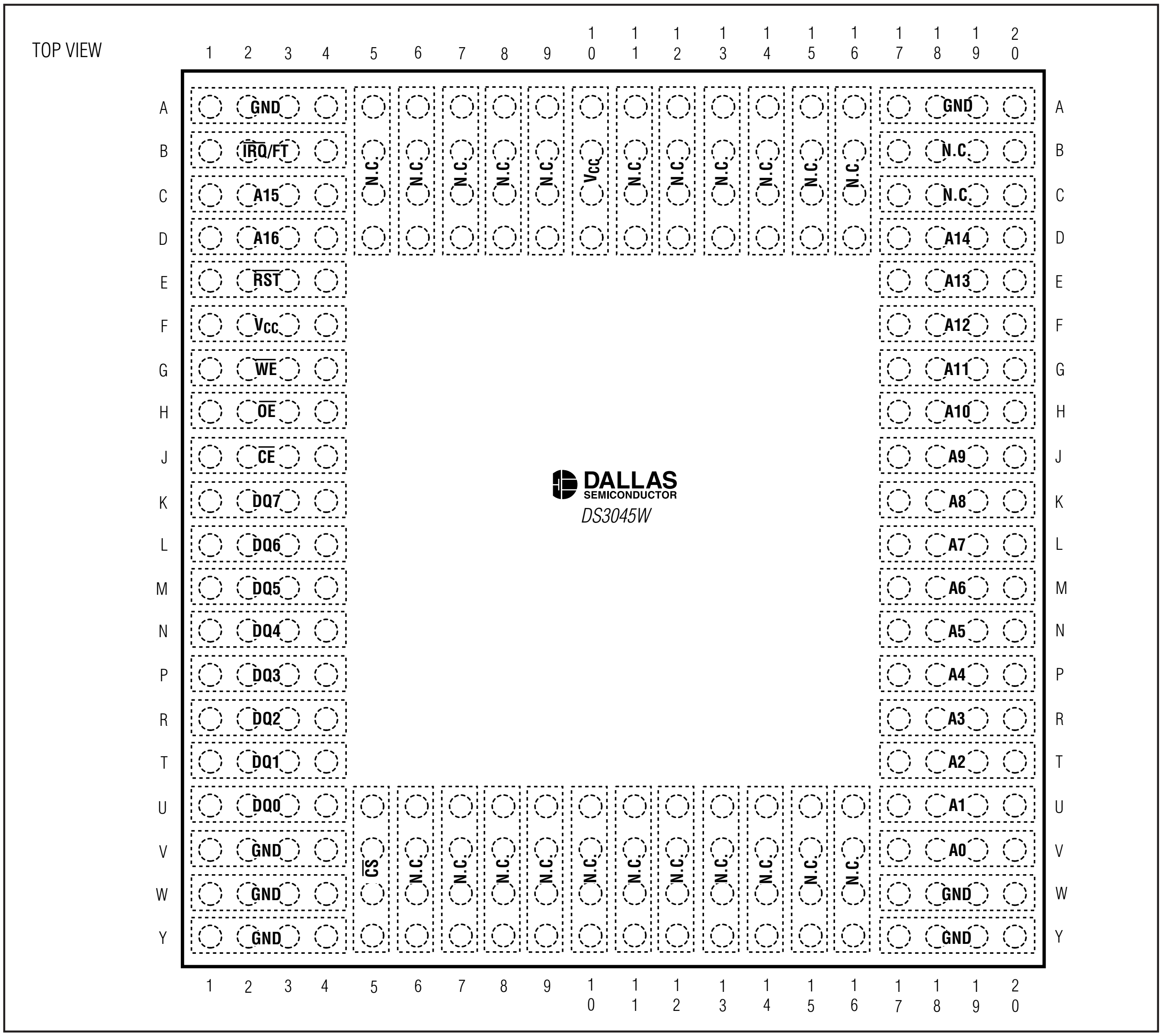


Figure 4. SRAM/RTC Data Bus Control

Pin Configuration



Revision History

Pages changed at Rev2: 1, 3, 4, 18

Package Information

For the latest package outline information, go to **www.maxim-ic.com/DallasPackInfo**.

DS3045W BGA modules are recognized by Underwriters Laboratory (UL) under file E99151.